(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 March 2002 (28.03.2002)

PCT

(10) International Publication Number
WO 02/24570 A1

(51) International Patent Classification[7]: B81C 1/00, B81B 3/00, 7/02

(21) International Application Number: PCT/GB01/04271

(22) International Filing Date: 25 September 2001 (25.09.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0023477.3 25 September 2000 (25.09.2000) GB

(71) Applicant *(for all designated States except US)*: **MARCONI CASWELL LIMITED** [GB/GB]; One Bruton Street, London W1J 6AQ (GB).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **BRIERLEY, Crofton, John** [GB/GB]; Estria, Fosters Booth Road, Pattishall, Northampton NN12 8JU (GB). **NEEDHAM, Anthony, Patrick** [GB/GB]; The Old School House, Bell Lane, Byfield, Northants NN11 6US (GB).

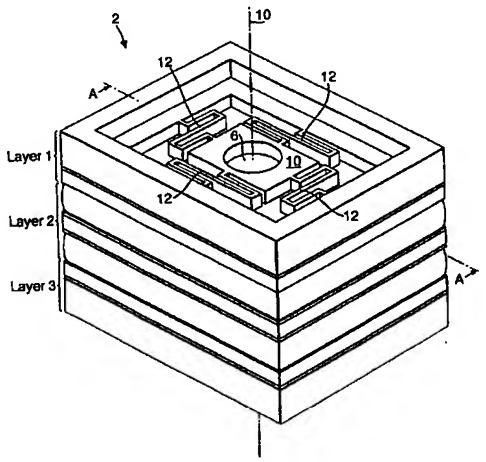
(74) Agent: **COCKAYNE, Gillian**; Marconi Intellectual Property, Marrable House, The Vineyards, Great Baddow, Chelmsford, Essex CM2 7QS (GB).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: MICRO ELECTRO-MECHANICAL SYSTEMS



(57) Abstract: A method of fabricating a micro electro-mechanical system device comprises: providing at least two layered wafers; selectively etching layers of said wafers and joining the etched wafers to form the device. One or more of said wafers comprises at least two material layers which, when selectively etched, form a part of the assembled device, said material layers having a layer of a different material therebetween which is resistant to an etchant of said material layers and wherein at least one of said material layers is of a pre-selected thickness which is used to define a spacing member for determining a distance between layers of the etched wafers when they are joined. The MOEMS devices may be for example micro-machined tiltable mirrors for use in optical cross connects in optical telecommunications, wavelength tuneable filters in the form of single etalon structures for selecting wavelength channels within wavelength division multiplex (WDM) optical signals, optical switches and variable optical attenuators for use is WDM optical telecommunications systems.

WO 02/24570 A1

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

MICRO ELECTRO-MECHANICAL SYSTEMS

This invention relates to micro electro-mechanical systems (MEMS) and more particularly to a method of fabricating such devices. More especially, although not exclusively, the invention concerns a tuneable optical filter for use in wavelength division multiplex (WDM) optical telecommunications system and a method for making the same.

MEMS are becoming more complex, particularly where such devices also contain an optical function (MOEMS) such as for example micro-machined tiltable mirrors for use in optical cross connects in optical telecommunications, wavelength tuneable filters in the form of single etalon structures for selecting wavelength channels within wavelength division multiplex (WDM) optical signals, optical switches and variable optical attenuators for use in WDM optical telecommunications systems to name but a few examples. For MOEMS the tolerances on dimensions, flatness, positional accuracy and parallelism of optical surfaces are crucial to the performance of the device. To accommodate the increasing complexity of these systems it is becoming necessary to fabricate the device from a number of wafers which are micro-machined and joined to form a layered assembly.

Depending on the particular device the cavities, or spaces, within or between the layers may need to be of the order of a few microns and up to 1 mm but with a tolerance that might be of the order of nanometres. Such accurate spaces over these relatively large dimensions cannot be easily defined using conventional spacing techniques like glue preforms or solder bonds. Neither can they be achieved by the deposition of materials

by evaporation, sputtering or electroplating, which are either only capable of thickness' of a few microns or impossible to control with sufficient accuracy in greater thickness'.

Most commonly MOEMS are fabricated using silicon micro-machining to provide the selected gaps between various thin film materials. In silicon micro-machining multiple layers of different materials are selectively deposited onto a flat substrate, such as a silicon wafer, such that the gaps separating each material are defined by the thickness of the intervening material. In an extension of this principle one or more of the intervening materials can be selectively removed (typically by chemical etching) to create an air gap of a distance defined by the removed material. One major limitation of deposition followed by a selective etching process, often termed surface micro-machining, is that nearly all thin film materials when deposited onto a different material have an intrinsic stress associated with them. Although this stress can be relieved when an underlying material is removed from the overlying material, this often results in a buckling or distortion in the overlying film (membrane) such that the dimension of the cavity created is not well defined. In applications which involve optical interactions such as, for example, an etalon, the membranes are required to be of exceptional flatness (sub nanometre) and to be aligned with exceptional parallelism relative to one another such that the gap can be adjusted with sub nanometre control by, for example, the application of an electrostatic or piezoelectric force.

In an attempt to reduce the likelihood of buckling or distortion of the membranes it is also known to fabricate MEMS by micro-machining silicon on insulator (SOI) wafers. As is known SOI technology was originally developed for fabricating high power

semiconductor devices and has subsequently been applied to the fabrication of MEMS. Typically an SOI wafer comprises a first layer of silicon, often termed handle layer, for handling the wafer during processing, an insulating layer, most often an oxide such as silicon dioxide, which acts as a buried etch stop when the wafer is used in the fabrication of a MEMS (rather than providing an electrically insulating layer as required in the fabrication of semiconductor devices) and a further silicon layer usually termed a device layer in which the device is formed. A particular advantage of using SOI for fabricating MOEMS is that since each silicon layer can be single crystal this results in them being substantially free of stress and consequently reduces the likelihood of buckling of the surfaces.

There are several methods of fabricating SOI wafers. One of the most common is to join two silicon wafers together in which one of the wafers is coated with silicon dioxide. Fusing of the wafers is achieved by firstly ensuring that both wafers are exceptionally flat and then pressing them together while being heated to an elevated temperature. This results, in a continuous bond between the silicon oxide coated silicon wafer and the pure silicon wafer. The silicon on one side of the silicon oxide barrier is then lapped and polished away to leave a thin layer (<2 μm – 100 μm) on one side (device layer) and a relatively thick layer on the other (handle layer).

SOI wafers have the advantage that the individual silicon layers are single crystal and substantially free of stress and that they may be readily etched in either a liquid or vapour, which has a high specificity for the silicon but very poor etching rate of the silicon oxide. Similarly the silicon oxide can be etched with chemical constituents

which have a very poor etch rate for pure silicon. By careful use of photolithographic masks, very precise structures can be machined into the silicon/silicon oxide layers.

In wavelength division multiplexed (WDM) optical communication a number of channels of information are carried on a single beam of light by combining a number of closely spaced wavelength channels. The conventional C band for instance has a bandwidth of 40 nm (1520 – 1560 nm) containing 32 channels of information each channel being 0.8 nm wide. At various points in the network it is required to select one or more channels and re-route them elsewhere. At present this is achieved by splitting the beam to pass into a number of separate optical fibres and providing a fixed wavelength filter at the output of each fibre which allows only one of the wavelength channels to pass. Thus each route can select only one channel. For current telecommunications systems there is a requirement to develop filters which are tuneable across the wavelength band of interest so that any one channel can be chosen from a single fibre providing optical flexibility.

One solution to this problem which has been proposed comprises a single cavity etalon filter. As is known such a device comprises two mirrors which are separated by a gap which is selected to be a finite number of wavelengths. For a given wavelength this gap is such that an optical resonance is created within the cavity between the two mirrors and that wavelength is able to pass through the mirrors. It is possible to tune the wavelength by varying the optical path length of the gap between the two mirrors either by modifying the refractive index of the medium between the two mirrors or by physically adjusting the gap between the two mirrors. The medium between the mirrors

may be a liquid, gas or vacuum provided it is substantially transparent at the wavelengths of interest. For the current and future spacing of the WDM channels this would require a cavity whose gap is very precisely defined and which can be adjusted with nanometre accuracy.

As described in our co-pending patent application GB 0003973.5, the content of which is hereby incorporated by way of reference thereto, the optical characteristics of an etalon filter can be improved by using a double cavity in which three mirrors are separated by two optical cavities. By physically adjusting the optical path length between the mirrors the optical shape of the filter can be significantly improved. This is achieved by the outer two mirrors being moveable. As described in our co-pending application such a filter enables any wavelength channel to be selected without needing to scan through intermediate channels.

The present invention arose in an endeavour to provide a method of fabricating a double cavity optical filter.

According to the present invention a method of fabricating a micro electro-mechanical system device comprises: providing at least two layered wafers; selectively etching layers of said wafers and joining the etched wafers to form the device; characterised by one or more of said wafers comprising at least two material layers which when selectively etched form a part of the assembled device, said material layers having a layer of a different material therebetween which is resistant to an etchant of said material layers and wherein at least one of said material layers is of a pre-selected

thickness which is used to define a spacing member for determining a distance between layers of the etched wafers when they are joined.

Preferably the material layers comprises silicon. and the etchant resistant layer comprises silicon dioxide.

According to a second aspect of the invention a micro electro-mechanical system device of a type comprising two or more layered wafers which have been selectively etched and joined together to form the device is characterised in that one or more of said wafers comprises at least two material layers which when selectively etched form a part of the assembled device, said material layers having a layer of a different material therebetween which is resistant to an etchant of said material layers and wherein at least one of said material layers is of a pre-selected thickness which is used to define a spacing member for determining a distance between layers of the etched wafers when they are joined.

Advantageously the one or more wafers comprises further material and etchant resistant layers and in which the further material layer is used to provide mechanical strength to the wafer and or assembled device.

Preferably the material layers comprise silicon and the etchant resistant layer comprises silicon dioxide.

The present invention finds particular application for devices which also involve an optical interaction and in a preferred embodiment the distance between layers defines an optical cavity.

In order that the invention can be better understood a tuneable optical filter fabricated in accordance with the invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a schematic isometric representation of a tuneable filter in accordance with the invention;

Figure 2 is a cross section through the filter of Figure 1 through a line "AA"; and Figures 3a – 3j illustrate various steps in the fabrication of the filter of Figures 1 and 2.

Referring to Figure 1 there is shown a tuneable optical filter 1 in accordance with the invention for use within a WDM optical telecommunication system for selecting a given wavelength channel. The filter 2 comprises a three layered structure in which the respective layers, denoted "layer 1", 2 and 3 in the Figure, are bonded together to form a filter assembly. As will be more readily appreciated from Figure 2 the filter comprises a double cavity etalon structure which is defined by a fixed central mirror 4 and two outer moveable mirrors 6 and 8. The fixed central mirror 4 is fabricated as part of layer 2 whilst the moveable mirrors 6 and 8 are formed as part of layers 1 and 3 respectively. As will be apparent from Figure 2 appropriate movement of the mirrors 6 and 8 relative

to the fixed mirror 4 and in a direction parallel with the optical axis 10 of the filter alters the dimensions of the two cavities and hence their resonance characteristic and thereby enables the filter to be selectively tuned to a desired wavelength channel. To enable movement of the mirrors 6, 8 each is mounted on a respective moveable support frame 10 which is formed as an integral part of the surrounding material and which is resiliently and deformably attached to the surrounding material by four flexible linkage arms 12 which have been formed by selectively etching through the material (Figure 1). Movement of the mirrors can be effected using a piezoelectric transducer which is conveniently deposited as a thin film and positioned on the linkage arms or using the electrostatic force generated between respective pairs of electrodes positioned on the support frames for the fixed and moveable mirrors. To ensure parallel movement of the mirrors 6, 8 four piezoelectric transducers or electrode pairs are provided for moving each mirror.

A method according to the invention for fabricating the filter 2 will now be described with reference to Figures 3a-3j, which illustrate various steps in the fabrication of the filter. Throughout these Figures, each of which is a cross section, the use of cross hatching has been deliberately omitted for reasons of clarity.

Referring to Figure 3a there is shown a silicon on oxide (SOI) wafer 14 which is used to fabricate the layers 1 and 3 of the filter. Layers 1 and 3 are identical and the following process steps accordingly apply to the production of both layers. The wafer 14 comprises a layered structure comprising, in order, a handle layer 16 of silicon (Si) which is used during fabrication to manipulate (handle) the wafer and to provide

mechanical strength once the wafer has been processed; a buried silicon dioxide layer 18 (SiO_2) which acts as an etch stop during micro-machining of the wafer and a device layer 20 of silicon in which the moveable support frame 10 and flexible linkage arms are to be formed. The device layer 20 is of a selected thickness with a very precise tolerance which is between 5 and 100 microns thick. The handle layer 16 can be any thickness appropriate to give mechanical support to the device and is typically 250 microns. The silicon layers 16, 20 and oxide layers are substantially stress free and each have a very high tolerance on their thickness and parallelism.

Referring to Figure 3b the moveable mirror 6, 8 is selectively deposited onto the surface of the device layer 20. Typically the mirror is a multilayer dielectric thin film material which is deposited using for example sputter deposition or other deposition technique.

Referring to Figure 3c the handle layer 16 is selectively etched to form a perimeter frame 22 which provides mechanical strength during subsequent processing of the wafer and allow acces to the buried oxide layer 18 for the next stage of fabrication. The frame 22 also provides a mechanical support for the completed filter such that it can be mounted and interconnected into a suitable package. It will be readily appreciated by those skilled in the art that any of the known micro-machining techiques can used during the processing of the wafers such as for example wet (chemical) or dry (plasma) etching.

Referring to Figure 3d using photolithography the oxide layer 18 and device layer 20 are selectively etched through their entire thickness to form the moveable support 10

and linkage arms 12. Finally the four piezoelectric actuators (not shown), in the form of a PZT film, are deposited on the linkage arms together with any metal layers required to allow electrical connection to the actuators. As described above in an alternative and preferred arrangement the support frame is moved electrostaically using elctrodes which are located around the perimeter of the support frame 10. In one embodiment it is also envisaged to additionally include piezoresistive or piezoelectric sensors on one or more of the flexible linkage arms to provide a measure of the strain and movement of the moveable support 10. Figure 3d represents the completed layers 1 and 3 of the filter.

Referring to Figure 3e there is shown a second SOI wafer 24 which is used to fabricate layers 2 of the filter which includes the fixed mirror 4. The wafer 24 unlike the known SOI wafers comprises a plurality of silicon device layers, three in the embodiment described, which are separated by a respective oxide layer. In order, the wafer 24 comprises: a handle layer 26 of silicon which is used during fabrication to manipulate (handle) the wafer; a first buried silicon dioxide layer 28 which acts as an etch stop during micro-machining of the wafer; a first device layer 30 of silicon into which spacing members (stand offs) will be formed for precisely defining the the dimension of the first cavity when layers 1 and 3 are subsequently joined; a second buried silicon dioxide layer 32 which acts as an etch stop during micro-machining of the wafer; a second device layer 34 of silicon in which a support frame for the fixed mirror 4 is formed; a third buried silicon dioxide layer 36 which acts as an etch stop during micro-machining of the wafer and a third device layer 38 of silicon in which spacing members (stand offs) will be formed for precisely defining the the dimension of the second cavity when the layer 1 is joined to the assembly. As with the first SOI wafer 14 each of the

device layers 30, 34, 38 are of a selected thickness of a very precise tolerance and are substantially stress free.

Referring to Figure 3f the device layer 38 of the second wafer is selectively etched to leave spacing members 40 (stand offs) extending from the surface of the wafer. It is to be noted that the spacing members 40, which can comprise a frame or a number of elements, extends from the wafer by an amount corresponding to the original thickness of the layer 38. The fixed mirror 4 is deposited in the form of a multi-layer dielectric film onto the surface of the third etch stop layer 36. Any electrical contacts as would be necessary for a filter which is to be operated electrostatically are appropriately deposited on the etch stop layer 36.

Referring to Figure 3g the partially processed second wafer (Figure3f) is inverted and joined to the processed layer 3 (Figure 3d) to provide essentially a single wafer for further processing. All further processing of the wafer assembly is conducted on the exposed surfaces of the second wafer and the perimeter frame 22 of layer 3 is used as the handle layer. The two wafers are joined together by means of an adhesive joint 42 around the periphery of the spacing members 40 though a solder joint could alternatively be used provided suitable wetting surfaces are provided. Whatever bonding technique is used it should ideally provide a tensile bond which pulls the two wafers together until the spacing members abut the surface of the layer 3. This is important since the gap between the opposing surfaces of the fixed mirror 4 and moveable mirror 6 (first optical cavity) is determined by the dimension of the spacing members 40.

Referring to Figure 3h the handle layer 26 is completely removed and the first device layer 30 selectively etched to leave second spacing members (stand offs) 44.

Referring to Figure 3i the second device and oxide layers 32, 34 are selectively etched through their entire thickness to define a frame which supports the fixed mirror 4. At this stage appropriate contacts can be set down as required especially where it is intended to operate the filter electrostatically.

Finally as shown in Figure 3j the completed layer 1 (Figure 3d) is inverted and bonded on top of the processed wafer assembly (Figure 3i) by means of adhesive joints 46 to form the finished optical filter assembly 2. As will be apparent from the Figure the gap between the opposing surfaces of the fixed mirror 4 and moveable mirror 8 (second optical cavity) is determined by the dimension of the spacing members 44.

It will be appreciated that the present invention is not limited to the optical filter described and that variations can be made which are within the scope of the invention. For example the method of using a layered wafer, most preferably an SOI wafer, having two or more device layers with a buried etch stop layer in between and micro-machining one or more of those device layers to provide spacing members such as to define very precise cavities and/or distances between layers of the machined wafers when the wafrs are subsequently joined is considered inventive in its own right and can accordingly be can be applied in the fabrication of any MEMS device. The present invention provides a method of fabricating and assembling a number of wafers such that gaps or spaces

between or within layers of the wafers are created that have a very well defined dimension, tolerance and parallelism. Since the thickness of the device layers of the SOI wafer are preselected when the wafer is made, this allows the spacing members and hence cavities to be created which have very precise dimensions. For example the thickness of the device layer used to create the spacing members could be as little as a fraction of a micron to many hundreds of microns, in either case the tolerence on the thickness being less than a micron across the entire wafer (up to 8 or more inches). This has a number of advantges in that thousands of identical devices all of which have the same dimensions and tolerances can be fabricated on a single wafer. Such dimensional accuracy is essential in applications in which the device operates at radio frequencies or involves optical interactions which can require accuracy in these dimensions which are a fraction of the wavelength of the radiation.

CLAIMS

1. A method of fabricating a micro electro-mechanical system device comprising: providing at least two layered wafers; selectively etching layers of said wafers and joining the etched wafers to form the device; characterised by one or more of said wafers comprising at least two material layers which when selectively etched form a part of the assembled device, said material layers having a layer of a different material therebetween which is resistant to an etchant of said material layers and wherein at least one of said material layers is of a pre-selected thickness which is used to define a spacing member for determining a distance between layers of the etched wafers when they are joined.

2. A method according to Claim 1 in which the material layers comprises silicon.

3. A method according to Claim 2 in which the etchant resistant layer comprises silicon dioxide.

4. A method of fabricating a micro electro-mechanical system device substantially as hereinbefore described with reference to and as illustrated in Figure 3a –3j of the accompanying drawings.

5. A micro electro-mechanical system device of a type comprising two or more layered wafers which have been selectively etched and joined together to form the device; characterised in that one or more of said wafers comprises at least two material layers which when selectively etched form a part of the assembled device, said material layers having a layer of a different material therebetween

which is resistant to an etchant of said material layers and wherein at least one of said material layers is of a pre-selected thickness which is used to define a spacing member for determining a distance between layers of the etched wafers when they are joined.

6. A device according to Claim 5 in which the one or more wafers comprises further material and etchant resistant layers and in which the further material layer is used to provide mechanical strength to the wafer and or assembled device.

7. A device according to Claim 5 or Claim 6 in which the material layers comprise silicon.

8. A method according to any one of Claims 5 to 7 in which the etchant resistant layer comprises silicon dioxide

9. A device according to any one of Claims 5 to 8 in which the distance between layers defines an optical cavity.

10. A tuneable optical filter substantially as hereinbefore described with reference to and as illustrated in Figures 1 and 2 of the accompanying drawings.

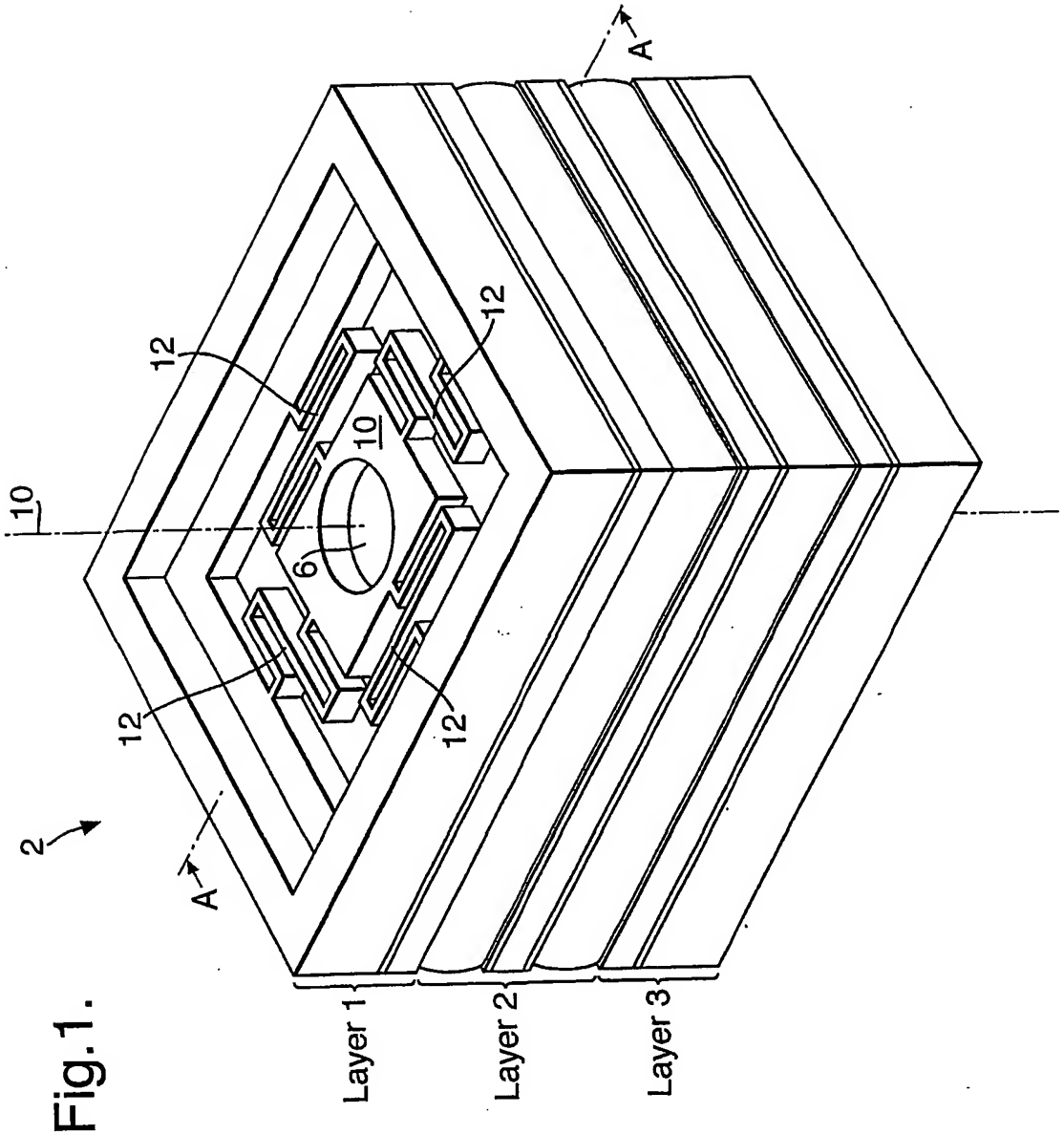


Fig.1.

Fig.2.

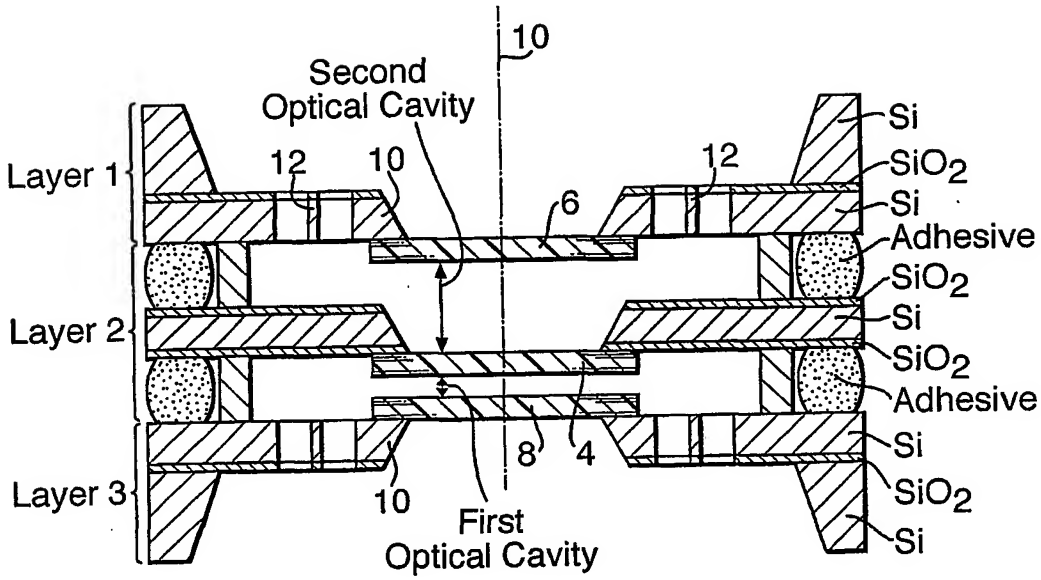

10
Second
Optical Cavity
Layer 1
Layer 2
Layer 3
12
10
6
12
8
4
10
First
Optical Cavity
Si
SiO2
Si
Adhesive
SiO2
Si
SiO2
Adhesive
Si
SiO2
Si

Fig.3a.

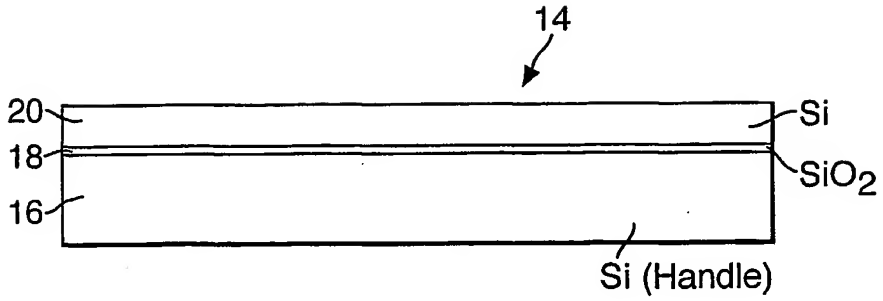


Fig.3b.

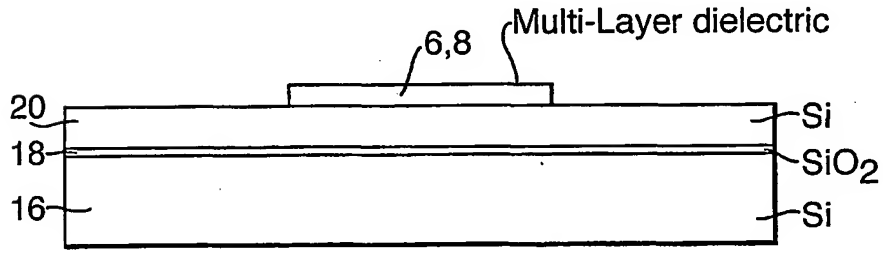


Fig.3c.

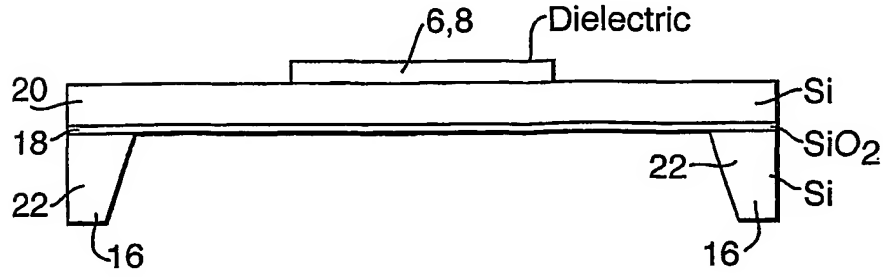


Fig.13d.

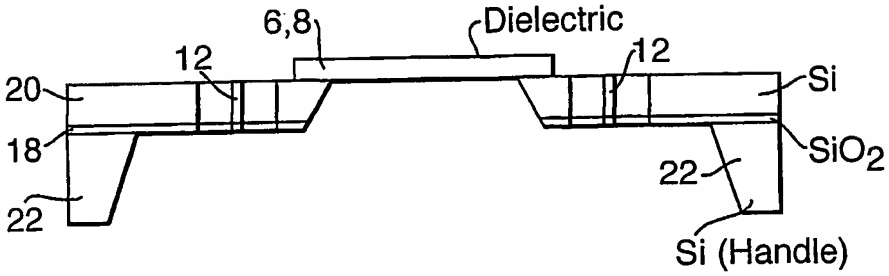


Fig.13e.

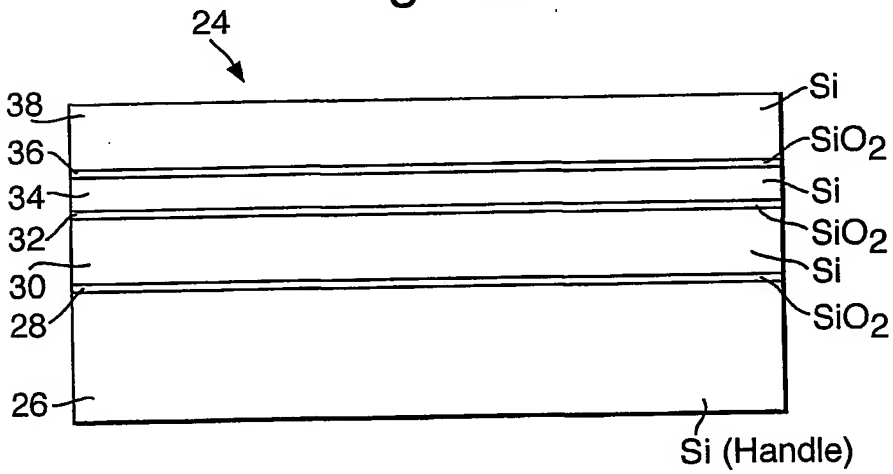


Fig.13f.

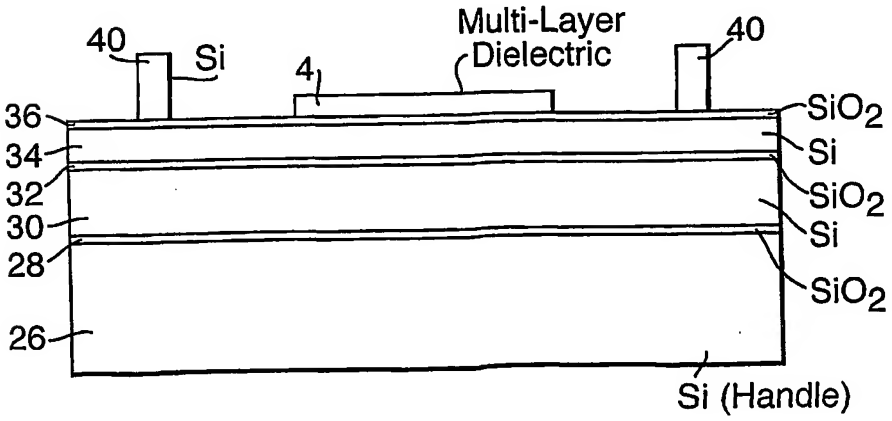


Fig.3g.

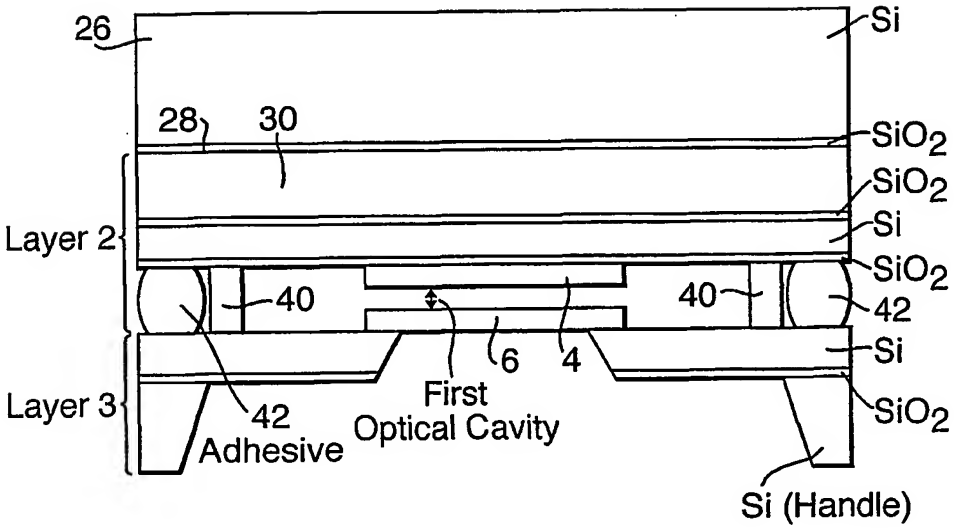

26
Si
28
30
SiO_2
SiO_2
Si
SiO_2
Layer 2
40
40
42
Si
6
4
Layer 3
42
First
Optical Cavity
SiO_2
Adhesive
Si (Handle)

Fig.3h.

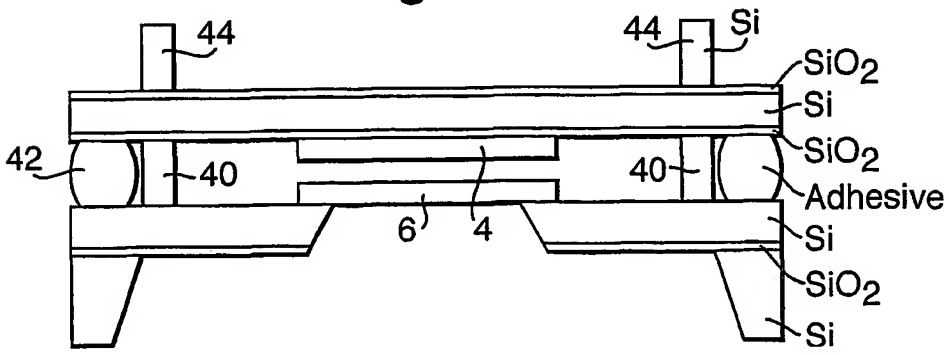

44
44
Si
SiO_2
Si
SiO_2
42
40
40
Adhesive
6
4
Si
SiO_2
Si

Fig.3i.

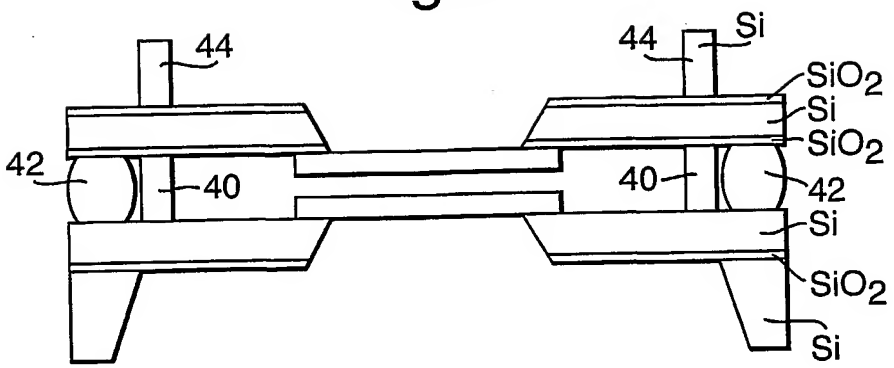
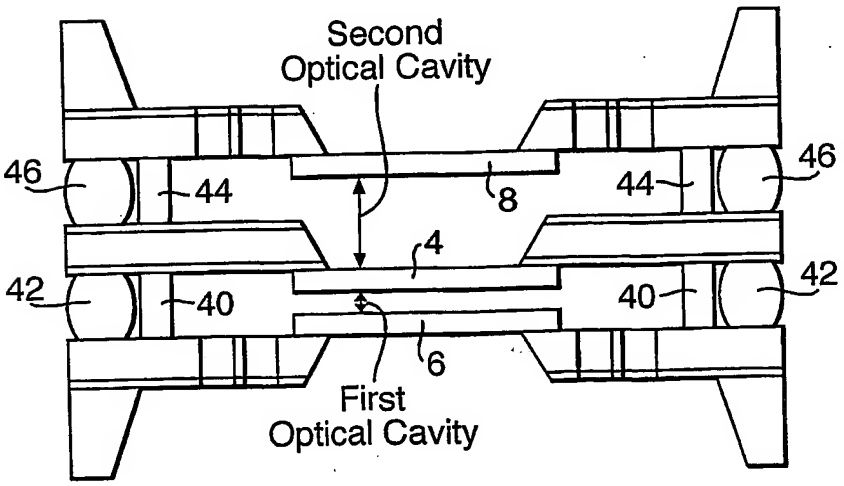

44
44
Si
SiO_2
Si
SiO_2
42
40
40
42
Si
SiO_2
Si

Fig.3j.


Second
Optical Cavity
46
44
8
44
46
4
42
40
40
42
6
First
Optical Cavity

INTERNATIONAL SEARCH REPORT

International Application No
PC', uB 01/04271

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B81C1/00 B81B3/00 B81B7/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81C B81B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 95 26567 A (I O SENSORS INC) 5 October 1995 (1995-10-05) figures 1-5 page 5, line 9 -page 6, line 16 page 8, line 21 -page 10, line 20	1-3,5, 7-9
A	——	6
X	US 5 344 523 A (FUNG CLIFFORD D ET AL) 6 September 1994 (1994-09-06) figures 2-5 column 2, line 42 -column 3, line 10 column 4, line 26 -column 7, line 15	1-3,5-8
A	——	1-3,5-9
	EP 0 502 222 A (HONEYWELL INC) 9 September 1992 (1992-09-09) figures 1-3 column 2, line 40 -column 5, line 27	
	——	
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2002	30/01/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Polesello, P

INTERNATIONAL SEARCH REPORT

Inter al Application No
PC.,/US 01/04271

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 488 862 A (NEUKERMANS ARMAND P ET AL) 6 February 1996 (1996-02-06) figures 5,6 column 6, line 9 - line 54 column 7, line 7 - line 26	1-3,5, 7-9
A	US 5 129 983 A (GREIFF PAUL) 14 July 1992 (1992-07-14) figure 3 column 3, line 34 -column 4, line 21	6

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 4,10

The subject matter of claim 4 is a method for fabricating a micro electro-mechanical system device substantially as hereinbefore described with reference to and as illustrated in Figure 3a-3j of the accompanying drawings.
The subject matter of claim 10 is a tunable optical filter as hereinbefore described with reference to and as illustrated in Figures 1 and 2 of the accompanying drawings.
Both the claims do not comply to Rule 6.2(a) of PCT and therefore are not allowed.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Inte ial Application No
PCT/GB 01/04271

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 9526567	A	05-10-1995	US	5484073 A	16-01-1996
			AU	2102195 A	17-10-1995
			CA	2159642 A1	29-09-1995
			EP	0700580 A1	13-03-1996
			JP	8511379 T	26-11-1996
			WO	9526567 A1	05-10-1995
US 5344523	A	06-09-1994	US	5323656 A	28-06-1994
			CA	2095783 A1	13-11-1993
			DE	69313716 D1	16-10-1997
			DE	69313716 T2	09-04-1998
			EP	0569899 A1	18-11-1993
			JP	6129933 A	13-05-1994
EP 0502222	A	09-09-1992	US	5006487 A	09-04-1991
			EP	0502222 A1	09-09-1992
			US	5115291 A	19-05-1992
US 5488862	A	06-02-1996	US	5629790 A	13-05-1997
			EP	0767915 A1	16-04-1997
			JP	9512904 T	22-12-1997
			WO	9524652 A1	14-09-1995
			US	5648618 A	15-07-1997
			US	6044705 A	04-04-2000
US 5129983	A	14-07-1992	NONE		